Ultrathin InGaO Thin Film Transistors by Atomic Layer Deposition

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***Abstract*— In this letter, we report on scaled ultrathin (~3 nm) InGaO (IGO) thin film transistors (TFTs) by atomic layer deposition (ALD) under a low thermal budget of 250 °C. The ALD-derived IGO channels are In-rich, with In/Ga atomic ratio of ~86:14, providing a high electron mobility of ~28.6 $cm^2 \cdot V^{-1} \cdot s^{-1}$ under a ultrathin thickness of 3 nm. The resulting IGO TFTs exhibit excellent scaling behaviors down to sub-100 nm channel length (L_{ch}). The IGO TFTs with a L_{ch} of 80 nm show well-behaved electrical characteristics including a high on/off current ratio (I_{on}/I_{off}) of 1.8×10^{10}, a low subthreshold swing (SS) of 92 mV/dec under V_{DS} of 0.8 V. The negative- and positive-gate-bias-stress stability (NBS and PBS) of IGO TFTs are studied in both N_2 and air ambient, where a remarkably high PBS stability can be observed. The negative V_{th} shifts during PBS and NBS test in N_2 ambient could be explained by the generation of donor-like traps originating from ionized oxygen vacancy, in addition to electron (de)trapping mechanism. This work presents the first demonstration of high-performance IGO TFTs with a miniatured device dimension, showing the potential for back-end-of-line (BEOL)-compatible monolithic 3D integration.**

***Index Terms*— Atomic layer deposition (ALD), thin film transistor (TFT), indium gallium oxide (IGO), reliability, back-end -of-line (BEOL).**

I. Introduction

INDIUM-BASED oxides have made a great success in traditional back-plane display due to their decent mobility, good uniformity, excellent optical transparency [1], [2], [3], [4], [5]. The high mobility of these In-based oxides could be explained by the isotopically spread In orbits overlap each other, providing an effective electron percolation path [1], [2]. Thus, pure In_2O_3 provide the highest mobility among oxides but suffer from degenerate carrier concentration and rich oxygen vacancy defects, thereby leading to high off-current (I_{off}) and device instability issues [2]. Doping In_2O_3 with other metal cation having a higher binding energy with oxygen has shown to be an effective method to resolve these issues in display applications [1], [2], [3], [4], [5]. Among these cation dopants, Ga with small radius, high ionic potential, and high bonding energy with oxygen is believed to be a strong oxygen binder and carrier suppressor to In_2O_3 [6], [7], [8], [9], [10], [11], [12]. In addition, crystalline Ga_2O_3 has similar edging-sharing octahedral structure as In_2O_3, thus the introduction of Ga would induce minimal distortions to In_2O_3 host structure and possibly maintain a high mobility. Some high-performance IGO TFTs has also been demonstrated in previous reports [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20]. However, these IGO TFTs were mainly aimed at display applications with channel thickness (T_{ch}) above 10 nm, channel length (L_{ch}) larger than 1 μm and process temperature typically above 400 °C. The scaled IGO TFTs with low thermal budget have not yet been demonstrated.

Recently, intensive attention has been garnered on applying oxide semiconductors for back-end-of-line (BEOL)-compatible logic and memory applications towards monolithic 3D integration [21], [22], [23]. High-performance scaled InGaZnO [21], InWO [22], In_2O_3 [23] TFTs have been demonstrated. Despite their excellent electrical performances, the stability of these scaled TFTs have not been carefully examined yet. It is generally believed that the electron (de)trapping at interface causes the V_{th} instability during gate-bias-stress test [24]. However, the high-electric field in scaled TFTs may accelerate the defect generation, adding a new mechanism to the V_{th} instability. Furthermore, H_2O and O_2 from measurement environments should also be considered [25], [26].

In this work, we report on ultrathin (~3 nm) IGO TFTs by atomic layer deposition (ALD) within 250 °C. The resulting IGO TFTs exhibit excellent scaling behaviors down to sub-100 nm L_{ch}. The IGO TFTs with a L_{ch} of 80 nm exhibit an I_{on}/I_{off} of 1.8×10^{10}, a SS of 92mV/dec under V_{DS} of 0.8 V. The negative- and positive-gate-bias-stress stability (NBS and PBS) of IGO TFTs are studied in both N_2 and air ambient, where a remarkably high PBS stability can be observed in both ambient. The negative V_{th} shifts during PBS and NBS test in N_2 ambient could be explained by the generation of donor-like traps originating from ionized oxygen vacancy, in addition to electron (de)trapping mechanism. This work presents the first demonstration of IGO TFTs with a miniatured device dimension and high PBS stability, showing a great promise for BEOL monolithic 3D integration.

II. Experiment

Figure 1(a) illustrates the schematic of the IGO TFTs, where 40 nm Ni, 6 nm HfO_2 and 3 nm IGO function as electrodes, dielectric, and semiconductor channel, respectively. The device fabrication process is largely similar to our previous work [23]. Briefly, an 8 nm Al_2O_3 was first deposited by ALD at 175 °C on the Si/SiO_2 substrates to obtain a smooth surface. Then, 40 nm Ni bottom gates were deposited

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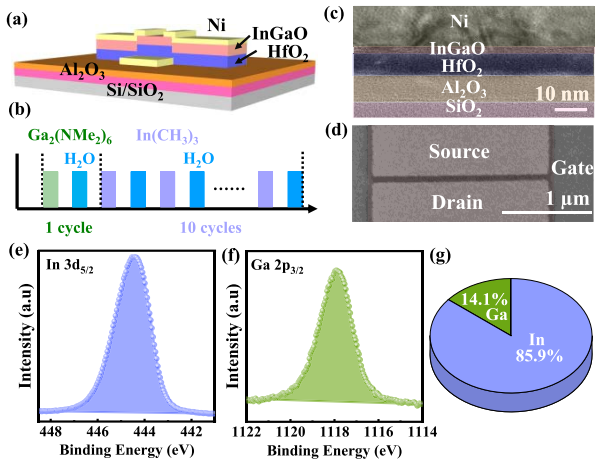

Fig. 1. (a) Device schematic; (b) Illustration of ALD growth; (c) False-color cross-sectional TEM image; (d) Top-view SEM image; (e) In $3d_{5/2}$XPS spectrum; (f) Ga $2p_{3/2}$XPS spectrum; (f) In/Ga atomic ratio.

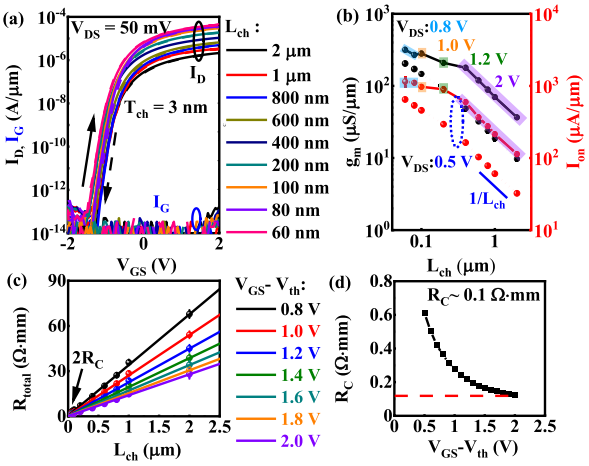

Fig. 2. (a) Transfer characteristics and gate leakage current (I_G) of IGO TFTs with L_{ch} ranging from 2 μm to 60 nm under V_{DS} of 50 mV. (b) Statistical results of g_m and I_{on} of IGO TFTs as a function of L_{ch} under V_{DS} of 0.5 V and under maximum V_{DS}. (c) Transfer length method measurements of IGO TFTs. (d) Extracted contact resistance (R_C).

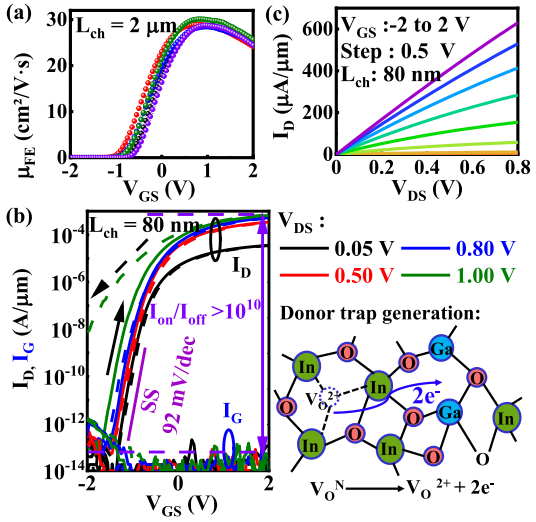

Fig. 3. (a) The extracted μ_{FE} from g_m based on five IGO TFTs with L_{ch} of 2 μm. (b) Transfer characteristics under various V_{DS} of IGO TFTs with a L_{ch} of 80 nm (Insets: the possible origin of donor trap generation, explaining the change of hysteresis direction); and (c) the corresponding output characteristics.

by e-beam evaporation, defined by photolithography. Next, 6 nm HfO_2 was deposited by ALD at 200 °C, followed by the deposition of 3 nm IGO by ALD at 225 °C. The IGO deposition started with one cycle of Ga_2O_3 followed by 10 cycles of In_2O_3, forming one super-cycle of the IGO growth (Fig.1(b)). A longer pulse time were adopted for In_2O_3 cycle compared to that of Ga_2O_3 cycle due to a weaker reactivity of In precursor. The IGO thickness is linearly increased with super-cycle numbers with a growth rate of ~1.25 Å/super-cycle, confirming the ALD growth nature. Then, IGO mesas were formed by BCl_3/Ar dry etching. Finally, 40 nm Ni was deposited as source/drain contacts by e-beam evaporation, defined by electron beam lithography. The fabricated TFTs have a channel width (W_{ch}) of 2 μm and a L_{ch} ranging from 2 μm to 60 nm. These IGO TFTs were subjected to O_2 annealing for 1 min at 250 °C after fabrication. Mild oxidization was adopted to prevent the oxidization of Ni contact, which could still leave some oxygen defects in IGO channel. Figure 1(c) shows the cross-sectional TEM image of IGO TFTs, where the thickness of each layer could be confirmed. Top-view SEM image of a typical IGO TFTs with a L_{ch} of 80 nm could be seen in Fig.1(d). The high In/Ga atomic ratio of 86:14 was confirmed by XPS in Figs. 1(e)-(g), which is beneficial for achieving a high μ_{FE}. Some N and C contamination can also be detected from XPS (not shown), which may come from the precursor ligand during growth.

III. Results and Discussion

Figure 2(a) shows bi-directional transfer characteristics of IGO TFTs with L_{ch} ranging from 2 μm to 60 nm under V_{DS} of 50 mV. All TFTs exhibit similar switching behaviors including high I_{on}/I_{off}, steep SS, similar V_{th}, and negligible hysteresis, indicating its immunity to the short channel effects down to 60 nm, benefiting from the excellent electrostatic control using the ultrathin gate stack. Figure 2(b) presents the statistical results of transconductance (g_m) and I_{on} of IGO TFTs as a function of L_{ch} under V_{DS} of 0.5 V and under maximum V_{DS} before severe self-heating occurs [27]. At least 5 devices of the same L_{ch} were measured for the average extraction and small error bars suggests the excellent uniformity of IGO channel. Both g_m and I_{on} follow the $1/L_{ch}$ trend under the same V_{DS}, which again suggests excellent scaling behavior of the ultrathin IGO TFTs. The contact resistance (R_C) can be extracted from TLM analysis (Fig.2(c)). A low R_C value of ~ 0.1 Ω·mm can be obtained under a gate overdrive (V_{GS}-V_{th}) of 2 V in Fig.2(d).

Figure 3(a) shows the extracted μ_{FE} of 28.6 ± 1.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$ from five TFTs with L_{ch} of 2 μm. The oxide capacitance (C_{OX}) of 1.65 $\mu F/cm^2$ were used for the extraction. Figure 3(b) exhibits transfer curves of a representative IGO TFTs with L_{ch} of 80 nm under various V_{DS}. An I_{on}/I_{off} of 1.8×10^{10} and a steep SS of 92 mV/dec can be observed under V_{DS} of 0.8 V. The V_{th} of −0.24 V can be extracted from the linear extrapolation of transfer curve under V_{DS} of 50 mV (not shown).

It is interesting to note that the hysteresis direction transit from clockwise to counterclockwise with increased V_{DS} in Fig.3(b). The clockwise hysteresis is generally explained by the electron-trapping at the interface while mobile positive ions could lead to a counterclockwise hysteresis [28]. In-rich

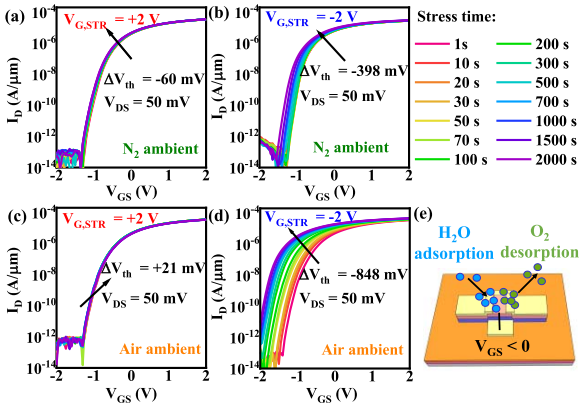

Fig. 4. Evolution of transfer characteristics in log-scale of IGO TFTs with L_{ch} of 80 nm under gate stress voltage ($V_{G,STR}$) of (a) +2 V; (b) −2 V in N_2 ambient; and (c) +2 V; (b) −2 V in air ambient for a stress time of 2000 s. (e) Schematic illustration of the environmental effects on the gate bias stability.

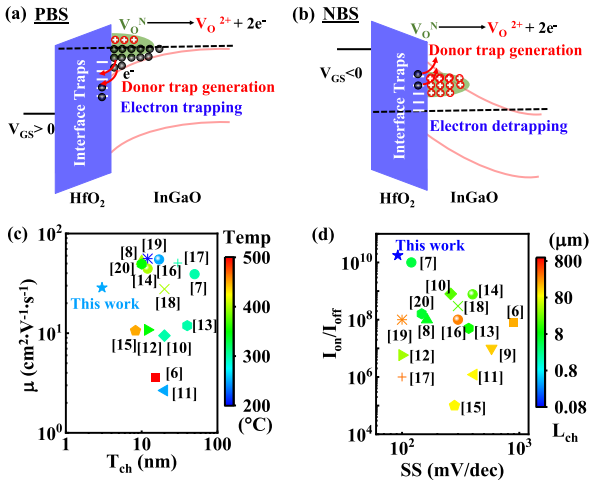

Fig. 5. Possible processes during (a) PBS test; and (b) NBS test, where donor-like traps could be generated from the ionized VN O in addition to electron trapping and de-trapping. These donor-like traps would have more significant effects during NBS test due to the electron depletion. (c) The comparison of the μ versus T_{ch} and process temperature; and (d) I_{on}/I_{off} versus SS and L_{ch} of IGO TFTs in this work with those from literatures.

oxides are well known to be rich of oxygen vacancy, which should be the case for our IGO films. These oxygen vacancies could work as shallow donor, where its charge transition levels (neutral to +2 positive charged) should locate at the edge of or in the conduction band of IGO, so called "negative-U" defects [29]. The neutral oxygen vacancy (V_O^N) could function as electron traps [30], explaining the clockwise loop at low V_{DS}. Under high electric field, these V_O^N defects could be ionized, releasing two electrons into conduction band and forming positive charged V_O^N in the channel and at the interface (Fig.3(b)), which lead to the counterclockwise loop. Negligable hysteresis is observed in bi-directional sweeps on long channel devices since the lateral electric field is much smaller. The corresponding output characteristics of the IGO TFT can be seen in Fig.3(c), where a high I_{on} of ~600 μA/μm is achieved under a V_{DS} of 0.8 V and a V_{GS}-V_{th} of ~2 V, which is among the best values reported for oxide TFTs [21], [22], [23]. Note that the V_{DS} is limited to 0.8 V for a stable device operation.

Gate bias stress stability tests were performed on the IGO TFTs with a L_{ch} of 80 nm under gate stress voltage ($V_{G,STR}$) of ±2 V in both N_2 and air ambient at room temperature (Fig.4(a)-(d)). During the stress test, the gate was biased at the given voltage while source and drain were grounded. The gate stress was interrupted to collect transfer curves under V_{DS} of 50 mV with a short integration time to avoid recovery and a short delay of 1 ms between measurement and stress. A remarkably high PBS stability can be observed in both ambient, with marginal ΔV_{th} of −60 mV in N_2 and +21 mV in air. For NBS test, TFTs show more a pounced negative ΔV_{th} of −848 mV in air compared to that of −398 mV in in N_2. The differences between air and N_2 ambient can be explained by the H_2O and/or O_2 adsorption/desorption from air in Fig.4(e). During NBS test, H_2O may be adsorbed on the IGO surface, donating some electrons to the channel, while O_2 may be desorbed from IGO surface, leaving extra electrons in the channel, both of which would cause a negative V_{th} shift [25]. Opposite process occurs for PBS test and such adsorption/desorption behavior could relate to the polarity of molecules [25]. This points out that a suitable passivation layer is necessary for our IGO TFTs. The recovery behavior of TFTs after NBS test were also studied by resting TFTs in N_2 ambient without applying any bias (not shown). The TFTs show very limited recovery after NBS in air in contrast to that a full recovery can be observed for those tested in N_2. The limited recovery after NBS test in air could be due to that the adsorption of H_2O molecules from air could be a chemical process related to surface contamination such as C and N [31], which could not be removed by resting in N_2.

The donor-like trap generation model is proposed to explain the observed ΔV_{th} shift in N_2 ambient. Under high electric field, V_O^N defects could be ionized, releasing two electrons into conduction band and leading to the negative V_{th} shift. During the PBS test, electrons were accumulated at channel/dielectric interface and a number of generated donor traps (V_O^{2+}) could be filled by these accumulated electrons, leading to a small negative V_{th} (Fig.5(a)). In the contrast, electrons were depleted during NBS test and these generated V_O^{2+} remain positively charged, resulting in a more pounced V_{th} shift (Fig.5(b)). After removing the bias, these ionized V_O^{2+} defects may capture the extra electrons and transit back to its neutral state through atomic reconstruction [32]. This may explain the full recovery behavior for TFTs tested in N_2 ambient. Figures 5(c) and (d) benchmark the IGO TFTs in this work with those from literatures [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20] in terms of T_{ch}, μ_{FE}, process temperature, I_{on}/I_{off}, SS and L_{ch}. To the best of our knowledge, this work presents the first demonstration of high-performance IGO TFTs with a miniatured device dimension and BEOL-compatibility.

IV. Conclusion

In summary, we report on ultrathin IGO TFTs enabled by ALD under a low temperature of 250 °C. The resulting IGO TFTs exhibit excellent scaling behaviors down to sub-100 nm. The IGO TFTs with a L_{ch} of 80 nm exhibit I_{on}/I_{off} of 1.8×10^{10}, SS of 92 mV/dec, and high PBS stability in both N_2 and air ambient. The negative V_{th} shifts during PBS and NBS test in N_2 ambient could be explained by the generation of donor-like traps originating from ionized oxygen vacancy, in addition to electron (de)trapping mechanism. This study demonstrates that ALD IGO TFTs have the potential for BEOL monolithic 3D integration.

REFERENCES

[1] T. Kamiya and H. Hosono, "Material characteristics and applications of transparent amorphous oxide semiconductors," *NPG Asia Mater.*, vol. 2, no. 1, pp. 15–22, Jan. 2010, doi: 10.1038/asiamat.2010.5.

[2] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *J. Display Technol.*, vol. 5, no. 7, pp. 273–288, 2009, doi: 10.1109/JDT.2009.2021582.

[3] Y. Shao, X. Xiao, X. He, W. Deng, and S. Zhang, "Low-voltage a-InGaZnO thin-film transistors with anodized thin HfO_2 gate dielectric," *IEEE Electron Device Lett.*, vol. 36, no. 6, pp. 573–575, Jun. 2015, doi: 10.1109/LED.2015.2422895.

[4] Y. Zhang, H. Yang, H. Peng, Y. Cao, L. Qin, and S. Zhang, "Self-aligned top-gate amorphous InGaZnO TFTs with plasma enhanced chemical vapor deposited sub-10 nm SiO_2 gate dielectric for low-voltage applications," *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1459–1462, Sep. 2019, doi: 10.1109/LED.2019.2931358.

[5] M. H. Cho, H. Seol, H. Yang, P. S. Yun, J. U. Bae, K. S. Park, and J. K. Jeong, "High-performance amorphous indium gallium zinc oxide thin-film transistors fabricated by atomic layer deposition," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 688–691, Mar. 2018, doi: 10.1109/LED.2018.2812870.

[6] J. H. Park, W. J. Choi, S. S. Chae, J. Y. Oh, S. J. Lee, K. M. Song, and H. K. Baik, "Structural and electrical properties of solution-processed gallium-doped indium oxide thin-film transistors," *Jpn. J. Appl. Phys.*, vol. 50, no. 8, Aug. 2011, Art. no. 080202, doi: 10.1143/JJAP.50.080202.

[7] K. Ebata, S. Tomai, Y. Tsuruma, T. Iitsuka, S. Matsuzaki, and K. Yano, "High-mobility thin-film transistors with polycrystalline In–Ga–O channel fabricated by DC magnetron sputtering," *Appl. Phys. Exp.*, vol. 5, no. 1, Jan. 2012, Art. no. 011102, doi: 10.1143/APEX.5.011102.

[8] Y. G. Kim, T. Kim, C. Avis, S. H. Lee, and J. Jang, "Stable and high-performance indium oxide thin-film transistor by Ga doping," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1078–1084, Mar. 2016, doi: 10.1109/TED.2016.2518703.

[9] Y. S. Rim, H.-W. Choi, K. H. Kim, and H. J. Kim, "Effects of structural modification via high-pressure annealing on solution-processed InGaO films and thin-film transistors," *J. Phys. D, Appl. Phys.*, vol. 49, no. 7, Jan. 2016, Art. no. 075112, doi: 10.1088/0022-3727/49/7/075112.

[10] J. Sheng, E. J. Park, B. Shong, and J. S. Park, "Atomic layer deposition of an indium gallium oxide thin film for thin-film transistor applications," *ACS Appl Mater Interfaces*, vol. 9, no. 28, pp. 23934–23940, Jul. 2017, doi: 10.1021/acsami.7b04985.

[11] W.-L. Huang, M.-H. Hsu, S.-P. Chang, S.-J. Chang, and Y.-Z. Chiou, "Indium gallium oxide thin film transistor for two-stage UV sensor application," *ECS J. Solid State Sci. Technol.*, vol. 8, no. 7, pp. Q3140–Q3143, Mar. 2019, doi: 10.1149/2.0251907jss.

[12] Y. Li, L. Lan, S. Hu, P. Gao, X. Dai, P. He, X. Li, and J. Peng, "Fully printed top-gate metal–oxide thin-film transistors based on scandium-zirconium-oxide dielectric," *IEEE Trans. Electron Devices*, vol. 66, no. 1, pp. 445–450, Jan. 2019, doi: 10.1109/TED.2018.2877979.

[13] M. Zhao, C. Song, Y. Xu, D. Xu, J. Zhang, T. Wu, R. Guo, and R. Chen, "Back-channel-etched oxide thin film transistors with a corrosion resistant crystalline InGaO channel," *ECS J. Solid State Sci. Technol.*, vol. 8, no. 4, pp. Q80–Q84, May 2019, doi: 10.1149/2.0191904jss.

[14] H. J. Yang, H. J. Seul, M. J. Kim, Y. Kim, H. C. Cho, M. H. Cho, Y. H. Song, H. Yang, and J. K. Jeong, "High-performance thin-film transistors with an atomic-layer-deposited indium gallium oxide channel: A cation combinatorial approach," *ACS Appl. Mater. Interface*, vol. 12, no. 47, pp. 52937–52951, Nov. 2020, doi: 10.1021/acsami.0c16325.

[15] G. Song, X. Zhang, J. Jiang, X. Sun, and H. Zheng, "Improved electrical performance of oxide transistor utilizing gallium doping both in channel and dielectric layers," *IEEE Electron Device Lett.*, vol. 41, no. 3, pp. 377–380, Mar. 2020, doi: 10.1109/LED.2020.2965138.

[16] S. H. Lee, S. Lee, S. C. Jang, N. On, H.-S. Kim, and J. K. Jeong, "Mobility enhancement of indium-gallium oxide via oxygen diffusion induced by a metal catalytic layer," *J. Alloys Compounds*, vol. 862, May 2021, Art. no. 158009, doi: 10.1016/j.jallcom.2020.158009.

[17] M. Furuta, K. Shimpo, T. Kataoka, D. Tanaka, T. Matsumura, Y. Magari, R. Velichko, D. Sasaki, E. Kawashima, and Y. Tsuruma, "7-4: High mobility hydrogenated polycrystalline In-Ga-O (IGO:H) thin-film transistors formed by solid phase crystallization," in *SID Symp. Dig. Tech. Papers*, vol. 52, no. 1, Jun. 2021, pp. 69–72, doi: 10.1002/sdtp.14612.

[18] T. Hong, H.-J. Jeong, H.-M. Lee, S.-H. Choi, J. H. Lim, and J.-S. Park, "Significance of pairing In/Ga precursor structures on PEALD $InGaO_x$ thin-film transistor," *ACS Appl. Mater. Interface*, vol. 13, no. 24, pp. 28493–28502, Jun. 2021, doi: 10.1021/acsami.1c06575.

[19] H. J. Park, T. Kim, M. J. Kim, H. Lee, J. H. Lim, and J. K. Jeong, "Improvement in performance of indium gallium oxide thin film transistor via oxygen mediated crystallization at a low temperature of 200 °C," *Ceram. Int.*, vol. 48, no. 9, pp. 12806–12812, May 2022, doi: 10.1016/j.ceramint.2022.01.151.

[20] M. H. Rabbi, S. Lee, D. Sasaki, E. Kawashima, Y. Tsuruma, and J. Jang, "Polycrystalline InGaO thin-film transistors with coplanar structure exhibiting average mobility of ≈78 $cm^2\ v^{-1}\ s^{-1}$ and excellent stability for replacing current poly-Si thin-film transistors for organic light-emitting diode displays," *Small Methods*, vol. 6, no. 9, Jul. 2022, Art. no. 2200668, doi: 10.1002/smtd.202200668.

[21] K. Han, Q. Kong, Y. Kang, C. Sun, C. Wang, J. Zhang, H. Xu, S. Samanta, J. Zhou, H. Wang, A. V.-Y. Thean, and X. Gong, "Indium-gallium-zinc-oxide (IGZO) nanowire transistors," *IEEE Trans. Electron Devices*, vol. 68, no. 12, pp. 6610–6616, Dec. 2021, doi: 10.1109/TED.2021.3113893.

[22] W. Chakraborty, H. Ye, B. Grisafe, I. Lightcap, and S. Datta, "Low thermal budget (<250 °C) dual-gate amorphous indium tungsten oxide (IWO) thin-film transistor for monolithic 3-D integration," *IEEE Trans. Electron Devices*, vol. 67, no. 12, pp. 5336–5342, Dec. 2020, doi: 10.1109/TED.2020.3034063.

[23] M. Si, Z. Lin, Z. Chen, X. Sun, H. Wang, and P. D. Ye, "Scaled indium oxide transistors fabricated using atomic layer deposition," *Nature Electron.*, vol. 5, no. 3, pp. 164–170, Feb. 2022, doi: 10.1038/s41928-022-00718-w.

[24] J.-M. Lee, I.-T. Cho, J.-H. Lee, and H.-I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 9, Sep. 2008, Art. no. 093504, doi: 10.1063/1.2977865.

[25] J. K. Jeong, H. W. Yang, J. H. Jeong, Y.-G. Mo, and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," *Appl. Phys. Lett.*, vol. 93, no. 12, Sep. 2008, Art. no. 123508, doi: 10.1063/1.2990657.

[26] K. Ide, Y. Kikuchi, K. Nomura, M. Kimura, T. Kamiya, and H. Hosono, "Effects of excess oxygen on operation characteristics of amorphous In-Ga-Zn-O thin-film transistors," *Appl. Phys. Lett.*, vol. 99, no. 9, Aug. 2011, Art. no. 093507, doi: 10.1063/1.3633100.

[27] P.-Y. Liao, M. Si, Z. Zhang, Z. Lin, and P. D. Ye, "Realization of maximum 2 A/mm drain current on top-gate atomic-layer-thin indium oxide transistors by thermal engineering," *IEEE Trans. Electron Devices*, vol. 69, no. 1, pp. 147–151, Jan. 2022, doi: 10.1109/TED.2021.3125923.

[28] N. Kaushik, D. M. A. Mackenzie, K. Thakar, N. Goyal, B. Mukherjee, P. Boggild, D. H. Petersen, and S. Lodha, "Reversible hysteresis inversion in MoS2 field effect transistors," *NPJ 2D Mater. Appl.*, vol. 1, no. 1, p. 34, Oct. 2017, doi: 10.1038/s41699-017-0038-y.

[29] A. de Jamblinne de Meux, A. Bhoolokam, G. Pourtois, J. Genoe, and P. Heremans, "Oxygen vacancies effects in a-IGZO: Formation mechanisms, hysteresis, and negative bias stress effects," *Phys. Status Solidi A*, vol. 214, no. 6, Mar. 2017, Art. no. 1600889, doi: 10.1002/pssa.201600889.

[30] H.-H. Nahm and Y.-S. Kim, "Undercoordinated indium as an intrinsic electron-trap center in amorphous $InGaZnO_4$," *NPG Asia Mater.*, vol. 6, no. 11, p. e143, Nov. 2014, doi: 10.1038/am.2014.103.

[31] Y.-S. Shiah, K. Sim, Y. Shi, K. Abe, S. Ueda, M. Sasase, J. Kim, and H. Hosono, "Mobility–stability trade-off in oxide thin-film transistors," *Nature Electron.*, vol. 4, no. 11, pp. 800–807, Nov. 2021, doi: 10.1038/s41928-021-00671-0.

[32] B. Ryu, H.-K. Noh, E.-A. Choi, and K. J. Chang, "O-vacancy as the origin of negative bias illumination stress instability in amorphous In–Ga–Zn–O thin film transistors," *Appl. Phys. Lett.*, vol. 97, no. 2, Jul. 2010, Art. no. 022108, doi: 10.1063/1.3464964.